Academic Year: 2018 -2019 (Ongoing)

Domain	S.No	Name of the Student	Guide Name	Title of the project
ANALOG CUSTOM IC DESIGN	01	DIVYA BARATHI A M KEERTHANA M SHIVARAMAKRISHNAN B	Dr. K. N. Vijeyakumar	DESIGN OF CURRENT FEEDBACK AMPLIFIER
	02	PARKAVI K GOKULA KANNA T SETHURAM S	Ms. S. Kalaiselvi	CMOS DESIGN OF INSTRUMENTATION AMPLIFIER
	03	DIVYA BARATHI A M KEERTHANA M SHIVARAMAKRISHNAN B	Dr. K. N. Vijeyakumar	ASIC DESIGN OF ENERGY EFFICIENT SUCCESSIVE APPROXIMATION ADC
DIGITAL CUSTOM IC DESIGN	01	SARANYA K GUNA JEEVITHA D NANTHINI K	Mr. B. Pradeepkumar	SINGLE-PRECISION FLOATION POINT FUSED-MULTIPLY-ADD ARCHITECTURE
	02	MONIKA P NAGASOWMIYA N GOWSALYA M	Dr. C. Kalamani	FPGA IMPLEMENTATION OF BORROW SAVE ADDER UNDER THRESHOLD VOLTAGE VARIABILITY
	03	CHITRA N JANANIPREETHA G R	Dr. K. N. Vijeyakumar	ASIC IMPLEMENTATION OF HIGH SPEED MULTIPLIER FOR DIGITAL IMAGE PROCESSING

	04	KARTHIK SRIDHAR R K DAYALAN S SHANMUGA PANDIAN J	Ms.S.Kalaiselvi	ASIC IMPLEMENTATION OF TRUNCATION-BASED APPROXIMATE MULTIPLIER
	05	GOWTHAM C SATHISH KUMAR M VIGNESH L	Ms. P.Sathyabama	VLSI DESIGN OF DIGIT BY DIGIT DECIMAL MULTIPLIER
	06	MALARVIZHI S NIHEETHA S AKSHAYA N	Dr.C.Kalamani	DESIGN AND IMPLEMENTATION OF POWER EFFICIENT SYNCRONOUS COUNTER
	07	SOORIYA PRAKASH N REVANTH P ARUN KUMAR S	Mr. B. Pradeep kumar	DESIGN OF HIGH SPEED 4-BIT MAC UNIT
	08	GOWRI PRASHANTH M SENTHUR SIVASAKTHIVEL C PRAVEEN KUMAR P	Ms. S.Kalaiselvi	VLSI ARCHITECTURE FOR CUBIC COMPUTATION USING VEDIC MATHEMATICS
	09	MONIKA P NAGASOWMIYA N CHITRA N RAMYA N	Dr.C.Kalamani	HIGH SPEED PARALLEL DECIMAL MULTIPLIER
	10	ARUNPRASANTH S MALLEESWARAN P	Mr. B. Pradeep Kumar	DESIGN OF LOWPOWER AND HIGH SPEED APPROXIMATE

				MULTIPLIER USING TREE COMPRESSOR
	11	ARUNKUMAR S KESAVAN M PRAVEEN KUMAR P GIRIPRASATH P	Ms. S.Kalaiselvi	ASIC IMPLEMENTATION OF ERROR TOLERANT UNSIGNED MULTIPLIER WITH CONFIGURABLE ERROR RECOVERY
FPGA Implementation of Image and Signal Processing Applications	01	KOWSALYA K ROHINI N KESAVAN M	Dr.K.N.Vijeyakumar	A FPGA BASED IMPLEMENTATION OF SOBEL EDGE DETECTION
	02	KOWSALYA K VEERA P NANDHAKUMAR S R	Dr.K.N.Vijeyakumar	A FPGA BASED IMPLEMENTATION OF APPROXIMATE COMPRESSOR BASED SOBEL EDGE DETECTION